6.334 Final Project – Buck Converter Design

By Tung Shen Chew

Overall Design

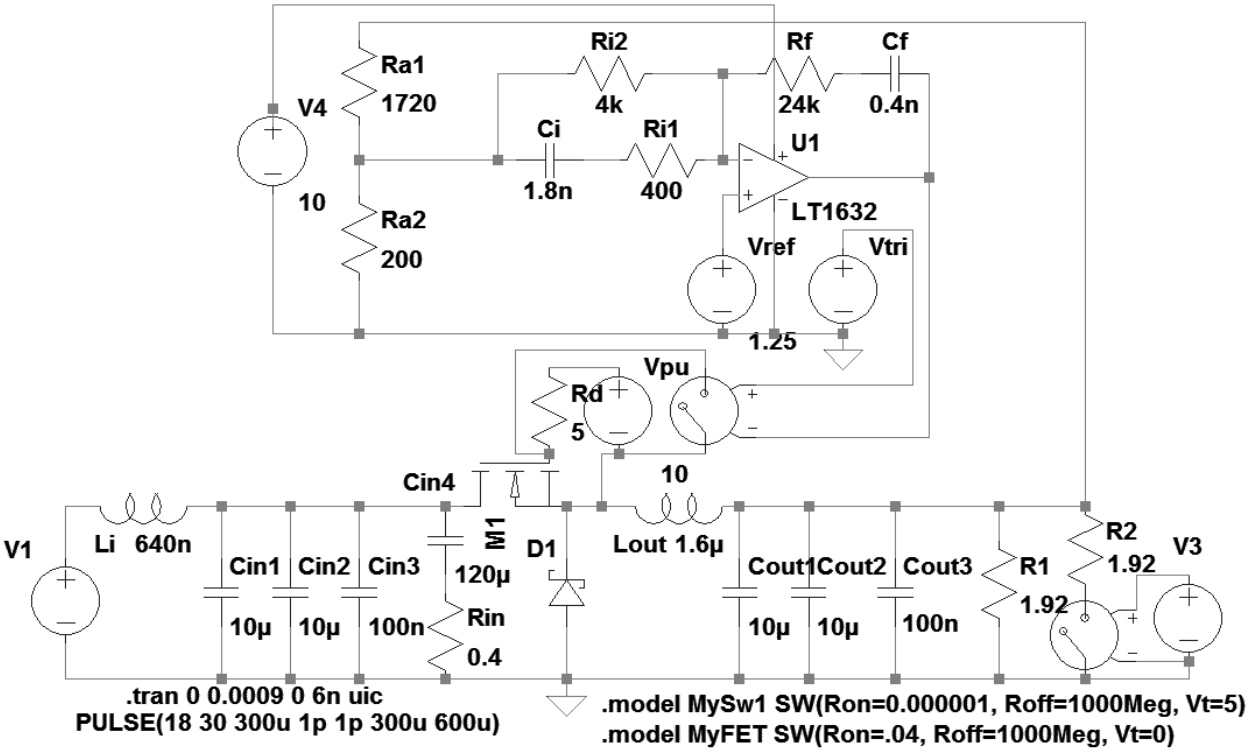

Figure 1: Overall circuit. Vtri and Vpu simulate a PWM gate driver.

Power Devices:	Mosfet:	IRFZ34N with KL50-1 heat sink
	Diode:	10TQ045 with ML26AA heat sink
Input Filter:	Inductor:	640nH, RM8/I-3F3-A160, 2 windings of 30 x 27AWG Litz wire
	Capacitors:	2 x 10uF Capstick + 100nF Panasonic-ECG (all parallel) 120uF Nichicon UHD1H121MHV
Output Filter:	Inductor:	1.6uH, RM8/I-3F3-A400, 2 windings of 45 x 27AWG Litz wire
	Capacitors:	2 x 10uF Capstick + 100nF Panasonic-ECG (all parallel)
Feedback:	Lead-compensated P+I controller implemented using LT1632 (45MHz UGBW)	
Switching Frequency:	600kHz	

Design Goals

Specification	Required	Calculated	Simulated
Input Voltage Range	18-30V	At least 18-30V	At least 18-30V
Input Voltage Transient Limit	44V for up to 1ms	All parts rated for >44V	-
Output Power Range	75-150W	At least 75-150W	At least 75-150W
Output Voltage (static)	12V ± 3%	12V ± 0% (P+I control)	12V ± 0.4%
Output Voltage (transient limits, varying load)	12V ± 20%	-	12V ± 6.8%
Allowed output voltage ripple (p-p, any load)	100mV	81mV	66mV
Allowed input current ripple (p-p, ideal source)	100mA	73mA	63mA
Minimum Efficiency	85%	90% (ignoring control & inductor losses)	-
Ambient Temp. Range	-20°C - +40°C	At least -20°C - +40°C	-

Table 1: Comparison of required, calculated and simulated specifications

In planning my approach for this project, I decided to give my design choices more direction by optimizing the buck converter for transient response. This meant choosing power devices which were as small as possible to cut down on switching losses. This would allow me to switch more often while keeping within the efficiency spec, allowing the use of smaller filter components and a higher filter cutoff frequency. The higher filter cutoff frequency allows the design of a feedback loop with a higher unity-gain bandwidth, improving the transient response of the buck converter. Since this approach encourages the use of smaller parts, it also helps keep down the cost of the design.

Choice of power devices

As mentioned above, the design is optimized for maximum switching frequency. This means that devices should be chosen which have relatively low switching losses at the expense of conduction losses, as the switching losses will dominate at higher frequencies.

Choosing the diode

The diode must be able to survive the maximum average diode current and the maximum input voltage (45V transient). Maximum average diode current is seen at maximum input voltage and output current, as the duty ratio will be at its lowest.

Using $V_{in} = 30V$, $D = 0.4$,

$$I_{out,max} = \frac{P_{out,max}}{V_{out}} = \frac{150W}{12V} = 12.5A$$

$$< I_{diode,max} > = I_{out,max} \cdot (1 - D_{min}) = 7.5A$$

Hence I chose the 10TQ045, a diode rated for 10A and 45V.

Choosing the Mosfet

Larger mosfets have higher switching losses due to higher output capacitance, gate charge and switching time. Hence I chose the smallest mosfet with an $R_{DS,on}$ which wouldn't cripple my efficiency. At minimum input voltage and maximum output current, the smallest mosfet available, the IRFZ24N, would have conductive losses of:

$$P_{cond,fet} = I_{out}^2 \cdot R_{DS,on} \cdot D_{max} = (12.5A)^2 \cdot (0.07\Omega) \cdot (0.67) = 7.33W$$

If I budget 10% of the input power to be dissipated in the power devices, this is over 40% of my active device power budget! As a result, I chose the next smallest mosfet, the IRFZ34N.

Having been unable to procure a good Spice model for the diode and mosfet, I substituted them in my simulation with models for a pair of devices with very similar electrical characteristics. These were the SI4480DY mosfet by Siliconix and the MBR20100CT diode by Motorola.

Switching Frequency

Budgeting 10% of my total power for dissipation in the diode and mosfet, I decided to calculate the overall dissipation of these two components as a function of switching frequency. This calculation was done at the corners of the input voltage and output power to ensure that I really did meet spec across all operating conditions.

Mosfet losses:

$$P_{sw,fet} = 0.5 \cdot (t_{rise} + t_{fall}) \cdot I_{out} \cdot V_{in} \cdot f_{sw}$$
$$P_{cond,fet} = I_{out}^2 \cdot R_{DS,on} \cdot D$$
$$P_{gate\ charge,fet} = Q_g \cdot V_{in} \cdot f_{sw}$$
$$P_{Cds,fet} = Q_{ds} \cdot V_{in} \cdot f_{sw} = \left(\sum C_{oss} \cdot \Delta V_{in} \cdot V_{in}\right) \cdot f_{sw}$$

Diode losses:

$$P_{cond,diode} = I_{out} \cdot V_{d,on} \cdot (1 - D)$$
$$P_{rev,diode} = I_{rev} \cdot V_{in} \cdot D$$
$$P_{charge,fet} = \left(\sum V_{in} \cdot \Delta V_{in} \cdot C_T\right) \cdot f_{sw}$$

Calculating and adding all these power losses over the four corners of input voltage and output power, I arrived at the following data:

Operating Conditions	$V_{in} = 18V$ $D = 0.67$	$V_{in} = 30V$ $D = 0.4$	Budgeted $P_{diss,fet} + P_{diss,diode}$	Maximum switching frequency
$P_{out} = 75W$ $I_{out} = 6.25A$	$(1.95 + 5.51\mu \cdot f_{sw})$	$(2.29 + 9.03\mu \cdot f_{sw})$	$8.5W$	680kHz
$P_{out} = 150W$ $I_{out} = 12.5A$	$(6.32 + 10.5\mu \cdot f_{sw})$	$(6.41 + 17.4\mu \cdot f_{sw})$	$17W$	608kHz

Table 2: Matrix of power dissipated in power devices over input voltage and output power

Based on this data, I concluded that 600kHz is the most appropriate switching frequency for this buck converter.

Heat sinks

Based on the 600kHz switching frequency chosen above, I would get a worst-case power dissipation in my devices of:

$$P_{diss,fet,max} = 12.8W$$
$$P_{diss,diode,max} = 4.05W$$

What is the smallest heat sink I could use to prevent the device junctions from exceeding 150°C at a maximum ambient temperature of 40°C?

Mosfet thermal calculation:

$$\begin{aligned} 150°C - 40°C = \; & P_{diss,fet,max} \cdot \left(R_{\Theta JC} + R_{\Theta CS} + R_{\Theta HS,fet}\right) \\ = \; & 12.8W \cdot \left(2.2\,{}^{\circ C}/_{W} + 0.5\,{}^{\circ C}/_{W} + R_{\Theta HS,fet}\right) \\ & R_{\Theta HS,fet} \leq 5.89\,{}^{\circ C}/_{W} \end{aligned}$$

I chose the KL50-1, with

$$R_{\Theta HS,fet} = 5.2\,{}^{\circ C}/_{W}$$

This results in a maximum junction temperature of 141°C.

Diode thermal calculation:

$$\begin{aligned} 150°C - 40°C = \; & P_{diss,diode,max} \cdot \left(R_{\Theta JC} + R_{\Theta CS} + R_{\Theta HS,diode}\right) \\ = \; & 4.05W \cdot \left(2\,{}^{\circ C}/_{W} + 0.5\,{}^{\circ C}/_{W} + R_{\Theta HS,diode}\right) \\ & R_{\Theta HS,diode} \leq 24.6\,{}^{\circ C}/_{W} \end{aligned}$$

I chose the ML26AA, with

$$R_{\Theta HS,diode} = 17.9\,{}^{\circ C}/_{W}$$

This results in a maximum junction temperature of 123°C.

Output Filter

The output filter is a 2nd-order LC low pass filter. We can expect the output voltage noise to be highest at maximum input voltage, so all the following calculations are done with $V_{in} = 30V$.

First of all, the inductor integrates the input voltage ripple created by the diode and mosfet. This integrated square wave voltage results in a triangle wave of current which is seen by the capacitor. Calculating the maximum peak-to-peak inductor current ripple:

$$i_{out,pp} = \frac{V_{in}}{2L_o} \cdot \frac{T}{2}$$

The capacitor then integrates this triangle wave of current, causing a quadratic variation in output voltage. Calculating the peak-to-peak amplitude of this voltage:

$$v_{out,pp} = \frac{1}{2} \cdot \frac{1}{C_o} \cdot \frac{i_{out,pp}}{2} \cdot \frac{T}{2} = \frac{V_{in} \cdot T^2}{32 \cdot L_o \cdot C_o} \leq 0.1V$$

$$L_o \cdot C_o \geq (26 \times 10^{-12})FH$$

I chose $C_o = 20uF$ because it was a conveniently large value (to improve transient load response) which could be obtained using the low-inductance Capstick capacitors. I later separated the 20uF into two 10uF Capstick capacitors in parallel with one high-frequency 100nF capacitor from Panasonic-ECG. This minimized the parasitic series inductance significantly, allowing good attenuation of my fairly high switching frequency.

Checking that the capacitor ripple current spec for each 10uF is not exceeded:

$$i_{Co,rms} = \frac{(\frac{i_{out,pp}}{2})^2}{12} = 0.23A \ll 15.3A\ max$$

I then chose $L_o = 1.6uH$ because it met the above constraint and was a convenient value easily met using two windings around an RM8/I-3F3-A400 inductor core. The core is wound with 45 strands of 27AWG Litz wire to carry high current at high frequency.

Checking that $B_{max} = 0.3T$ is not exceeded:

$$i_{Lo,max} = \frac{B_{max} \cdot A_{eff} \cdot N}{L_o} = \frac{(0.3T) \cdot (63mm^2) \cdot 2}{1.6uH} = 24A \gg 12.5A$$

It is worth noting that the output filter is satisfactorily damped by the load, and hence more filter damping at resonance using a resistor in series with a capacitor is not strictly required, although it prevents the circuit from exploding when the load is removed! If one is strictly required to prevent said explosion, I recommend 0.4Ω in series with a 120uF Nichicon UHD1H121MHV capacitor. This combination is used on the input filter to good effect.

Input Filter

The output filter is a 2nd-order LC low pass filter. It includes a small resistor in series with a large capacitor to provide resistive damping at the resonant frequency.

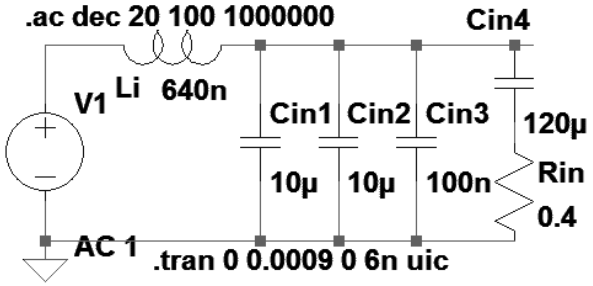

Figure 2: Input filter design

Finding the transfer function of input current to output current of the filter:

$$\frac{i_{in}}{i_{out}}(s) = \frac{1}{1 + s\frac{L_i}{R_{in}} + s^2 L_i C_i}$$

I then chose the LC constant of the filter to set how much it attenuated the fundamental frequency of the current ripple. Estimated worst-case output current ripple at 600kHz:

$$i_{out,fund,pp} = 12.5A \cdot \frac{4}{\pi} \cdot \frac{12V}{18V} = 10.6A$$

This requires an attenuation of roughly 41dB to meet the 100mA ripple spec. I thus placed the resonant LC frequency at 44.5kHz to achieve a 45dB attenuation of the 600khz fundamental. This was done with the same combination of capacitors as in the output filter, and a 640nH inductor with two windings around the RM8/I-3F3-A160 core. I met the high-frequency current carrying requirement using 45 strands of 27AWG Litz wire to minimize skin effect. In deciding the size of the damping resistor, I had to know the worst case input impedance of the buck converter:

$$z_{in} = \frac{dv_{in}}{di_{in}} = \frac{d}{di_{in}} \cdot \frac{P_{in}}{I_{in}} = -\frac{P_{in}}{v_{in}^2} = -\frac{v_{in}^2}{P_{in}} = -\frac{(30V)^2}{\frac{75W}{0.85}} = -10.2\Omega$$

I then chose the damping resistor to get less than 10dB of peaking:

$$R_{in} \cdot \sqrt{\frac{C_{in}}{L_{in}}} < \sqrt{10}$$

Thus I chose $R_{in} = 0.4\Omega$, which is so small that the negative impedance of the buck converter has negligible effect. It is in series with a 120uF Nichicon UHD1H121MHV capacitor to prevent it from loading the input filter at DC.

Feedback Design

My feedback controller is a proportional + integral controller with additional lead compensation. The integral component of the feedback allows for near-zero steady-state error, while the load compensation improves phase margin (and hence transient settling time) at the unity-gain frequency of the feedback loop. It is important to note that the gain of the feedback loop actually changes with the input voltage, as the PWM generator creates a gain in the loop of $\frac{V_{in}}{V_{pwm,pp}}$. Luckily, the input voltage changes over less than an order of magnitude, so the lead compensator is still a feasible means of creating additional phase margin. This is because the ≈45° of phase margin it creates is only over one order of magnitude in frequency. As I am principally an analog circuitry designer with a background in classical feedback, I thought it best to demonstrate my feedback transfer function with a circuit:

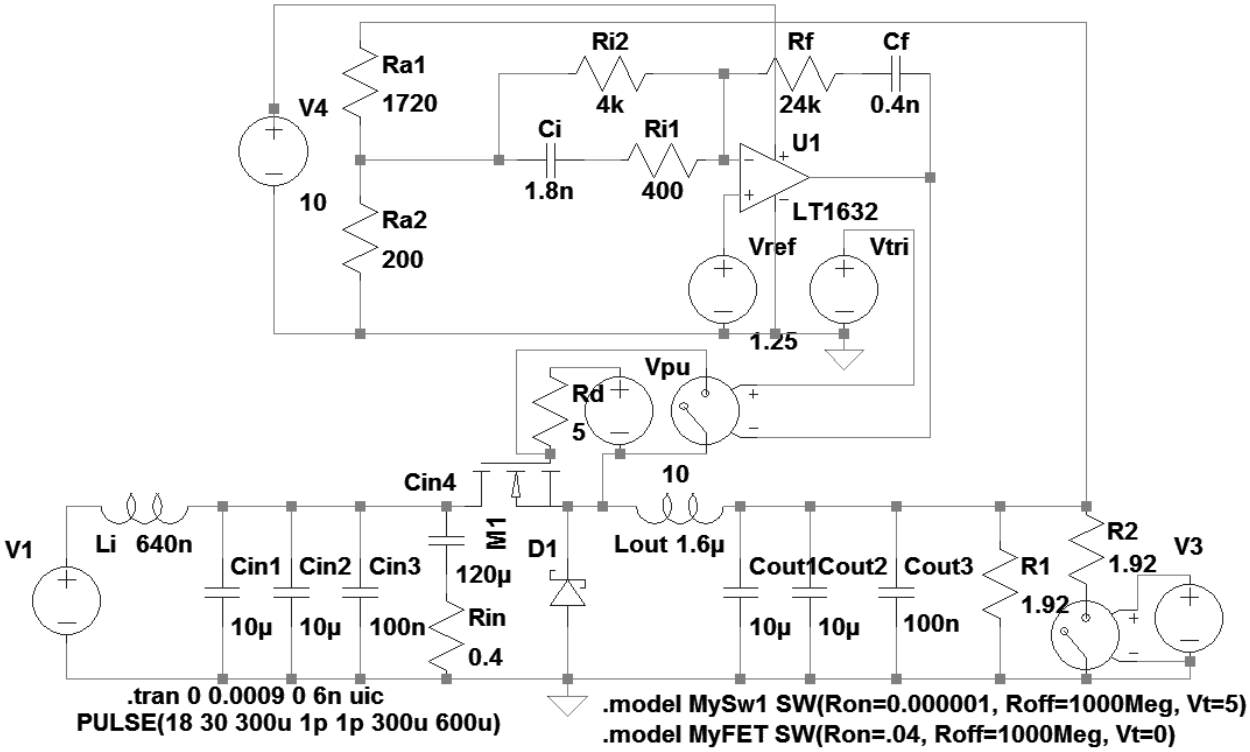

Figure 3: Overall circuit diagram repeated to show feedback circuitry

Resistors Ra1 and Ra2 divide down the 12V output to allow the circuit to compare it to the 1.25V bandgap voltage reference represented by Vref. In my simulations, a simple sine-triangle pulse-width modulator is creates by using Vtri as an ideal 600kHz 8Vpp triangle wave generator. This triangle wave is compared to the output of the op-amp using an ideal voltage-controlled switch and 5Ω pull-up resistor to represent a comparator and gate driver. In this simulation, another ideal switch is used to place an additional 1.92Ω resistor in parallel with the load resistor, allowing me to observe the transient response when the load current must suddenly

transition from 6.25A to 12.5A and vice-versa. The overall loop gain is represented by the following Bode plot:

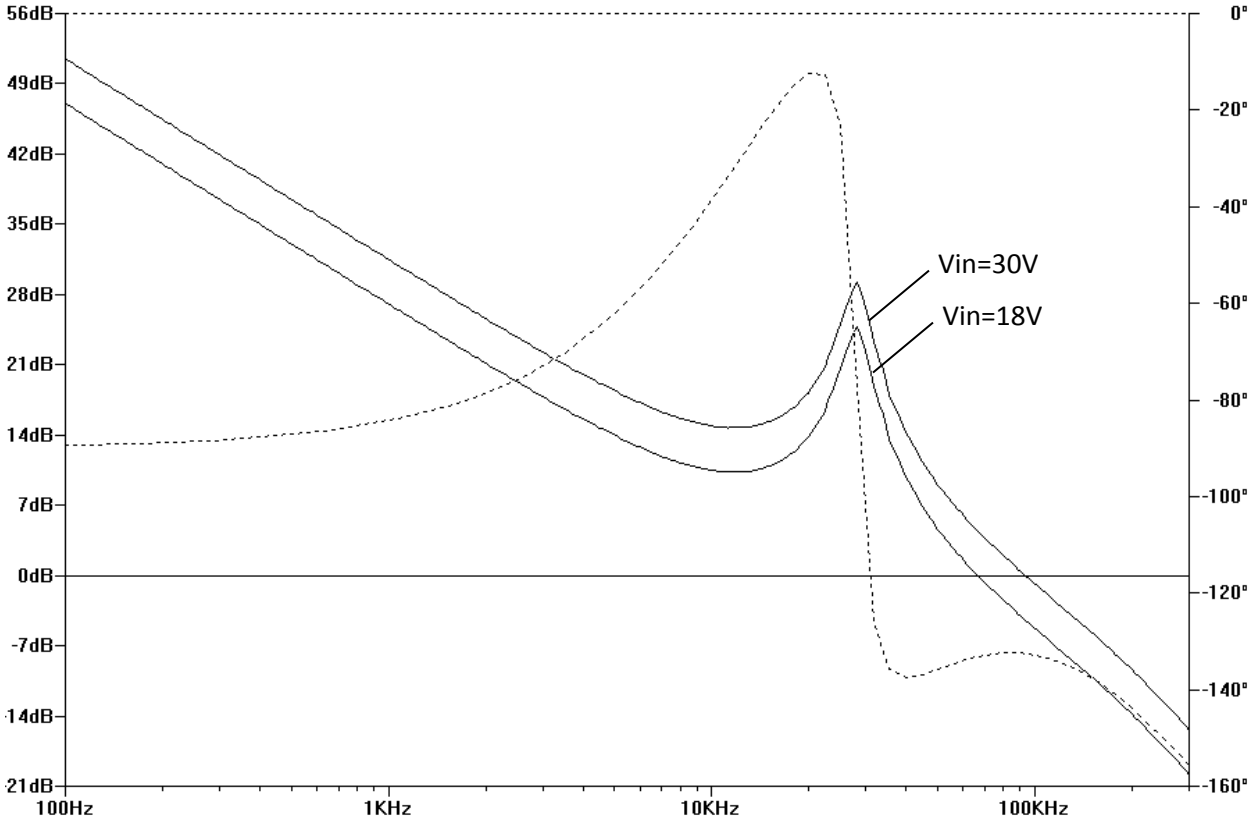

Figure 4: Bode plot of feedback loop gain

As can be seen in the Bode plot, different input voltages between 18V and 30V create a range of unity-gain frequencies from 66kHz to 93kHz. Across this range of frequencies, the phase shift is almost uniformly -135°, indicating a system with ≈45° of phase margin.

The proportional + integral characteristic is formed by Rf and Cf; Cf causes an integration until 16.6kHz, beyond which the frequency response flattens out. Without the lead network formed by Ri1, Ri2 and Ci, the 2nd-order output filter's dual poles at 28.1kHz would cause the unity gain bandwidth to range from 33kHz to 42kHz and the phase margin to be essentially zero. The lead network inserts a zero at 22.1kHz and a pole at 221kHz, roughly doubling the unity-gain bandwidth and granting 45° of phase margin.

I then simulated an instantaneous increase and decrease in output current (by inserting and removing another 1.92Ω resistor in parallel with the 1.92Ω load) to show the circuit's transient handling:

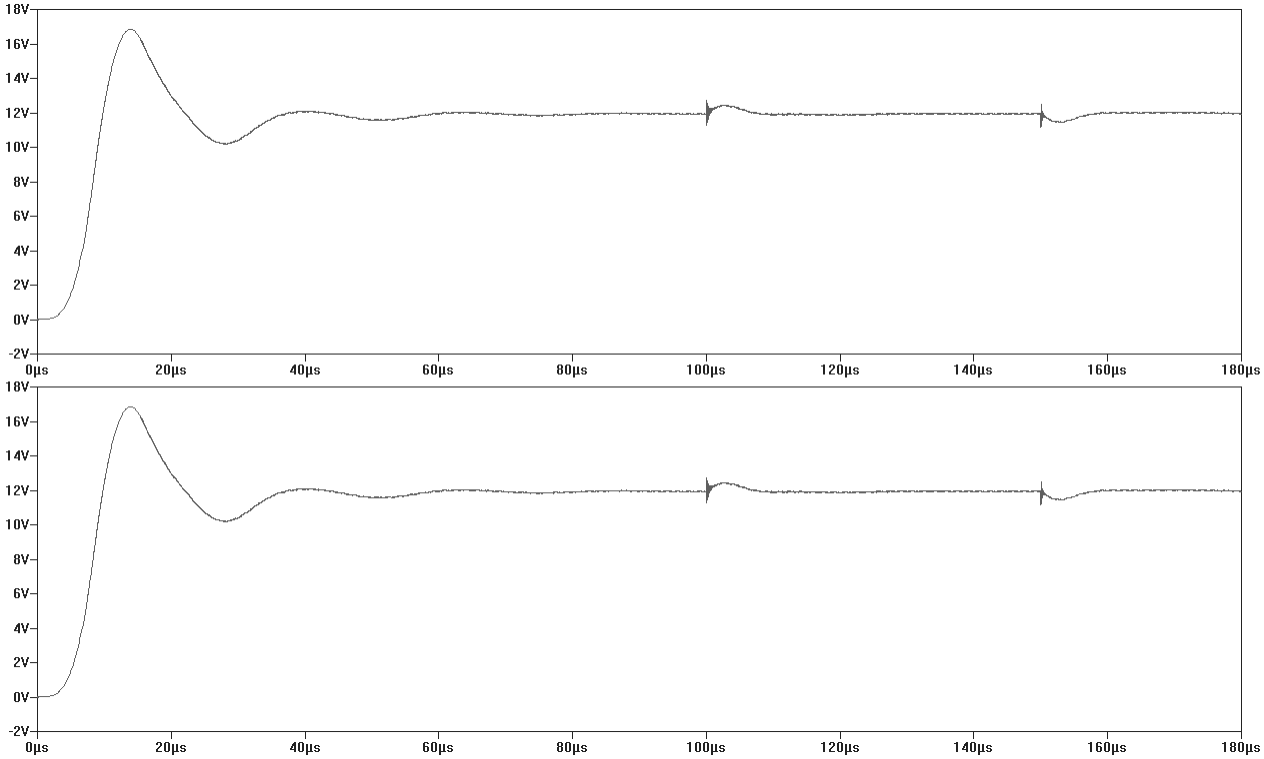

Figure 5: Turn-on & 6.25A/12.5A transient response for 18V(top) & 30V(bottom) inputs

As shown above, the worst-case transient response is ≈800mV peak deviation away from 12V. In all cases, the circuit returns to within static voltage spec (12V ± 3%) in under 8µs. The turn-on transient also meets static spec within 40µs.

Conclusion

As mentioned in the 'design goals' section, my personal goal was to take a somewhat lenient set of specs and optimize for transient response to the best of my ability. I think the result is reasonably good, although if I had more time I would have certainly tried incorporating minor-loop feedback. I've learned a lot. Thanks for a great class!